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AMERICAN SOCIETY FOR TESTING AND MATERIALS
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Standard Test Method for Characterization of Metal-Oxide-Silicon (MOS) Structures by Capacitance-Voltage Measurements [1]

This standard is issued under the fixed designation F 1153; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers procedures for measurement of metal-oxide-silicon (MOS) structures for flatband capacitance, flatband voltage, average carrier concentration within a depletion length of the semiconductor-oxide interface, displacement of flatband voltage after application of voltage stress at elevated temperatures, mobile ionic charge contamination, and total fixed charge density. Also covered is a procedure for detecting the presence of P-N junctions in the subsurface region of bulk or epitaxial silicon.

1.2 The procedure is applicable to *n*-type and *p*-type bulk silicon with carrier concentration from 5×10^{14} to 5×10^{16} carriers per cm^{3}, inclusive, and N/N^{+} and P/P^{+} epitaxial silicon with the same range of carrier concentration.

1.3 The procedure is applicable for test specimens with oxide thicknesses of 50 to 300 nm.

1.4 The procedure can give an indication of the level of defects within the MOS structure. These defects include interface trapped charge, fixed oxide charge, trapped oxide charge, and permanent inversion layers.

1.5 The precision of the procedure can be affected by inhomogeneities in the oxide or in the semiconductor parallel to the semiconductor-oxide interface.

1.6 The procedure is applicable for measurement of mobile ionic charge concentrations of 1×10^{10} cm^{-2} or greater. Alternative techniques, such as the triangular voltage sweep method [2] **(1)**, may be required where mobile ionic charge concentrations less than 1×10^{10} cm^{-2} must be measured.

1.7 The procedure is applicable for measurement of total fixed charge density of 5×10^{10} cm^{-2} or greater. Alternative techniques, such as the conductance method **(2)**, may be required where the interface trapped-charge density component of total fixed charge of less than 5×10^{10} cm^{-2} must be measured.

1.8 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

F 388 Method for Measurement of Oxide Thickness on Silicon Wafers and Metallization Thickness by Multiple Beam Interference (Tolansky Method) [3]

F 576 Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry [4]

F 723 Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon [4]

3. Terminology

3.1 *Definitions of Terms Specific to This Standard*:

3.2 *accumulation condition*—the region of the C-V curve for which a 5 V increment toward a more negative voltage for p-type material (Fig. 1), or toward a more positive voltage for *n*-type material (Fig. 2), results in less than a 1 % change in the maximum capacitance, C_{max}.

3.3 *equilibrium capacitance*—that capacitance reached after an MOS specimen at a fixed bias is illuminated and then allowed to stabilize in darkness.

3.4 *flatband condition, in microelectronics*—the point at which an external applied voltage causes there to be no internal potential difference across an MOS structure. Under practical conditions, metal-semiconductor work-function differences and charges in the oxide require the application of an external voltage to produce the flatband condition.

3.5 *flatband voltage*, V_{fb}—the applied voltage necessary to produce the flatband condition.

3.6 *flatband capacitance*, C_{fb}—the capacitance of an MOS structure at the flatband voltage.

3.7 *inversion condition*—for the purposes of this test method and for measurements on surfaces that do not exhibit a permanent inversion layer, the region of the Capacitance-Voltage, (C-V) curve for which a 5 V increment toward a more positive voltage for *p*-type material (Fig. 1), or toward a more negative voltage for *n*-type material (Fig. 2), results in less than

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[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] Boldface numbers in parentheses refer to the list of references at the end of this test method.

[3] Discontinued; see *1992 Annual Book of ASTM Standards*, Vol 10.05.

[4] *Annual Book of ASTM Standards*, Vol 10.05.

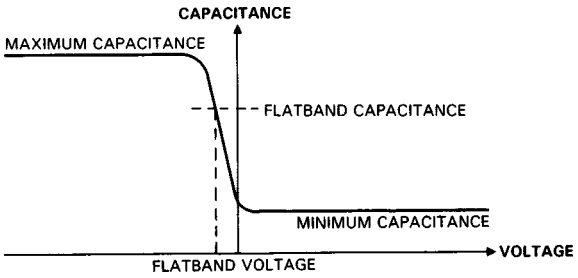


FIG. 1 Typical Capacitance-Voltage Plot of MOS Device Fabricated with *p*-Type Silicon

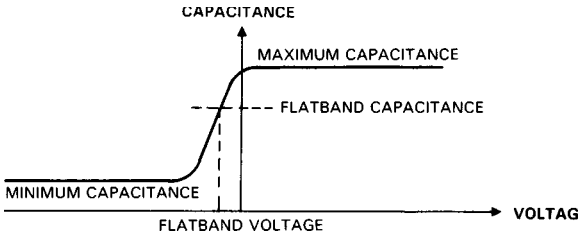


FIG. 2 Typical Capacitance-Voltage Plot of MOS Device Fabricated with *n*-Type Silicon

1 % change in the equilibrium minimum capacitance, C_{min}.

3.8 *permanent inversion layer*—for the purposes of this test method, the region of the C-V curve that exhibits a definite minimum ''dip,'' as shown in Fig. 3. The permanent inversion layer is an anomalous condition caused by interface charge or surface conditions and prevents proper determination of C_{min}.

3.9 *total fixed charge density, N_{tf}*—the sum of the nonmobile charge densities: oxide fixed charge density, oxide trapped charge density, and interface trapped charge density **(3)**.

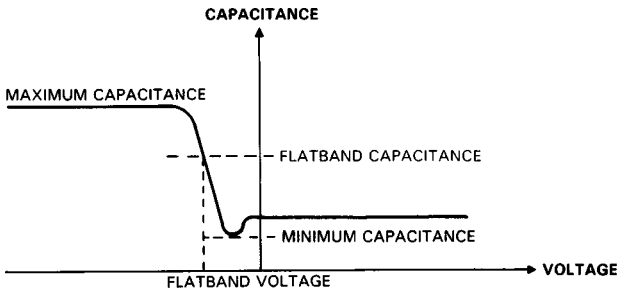
4. Summary of Test Method

4.1 A specimen MOS structure consisting of a metal field plate on the oxidized silicon substrate is fabricated.

4.2 The small-signal, high-frequency capacitance of the specimen is measured as a function of a ramped voltage applied between the field plate and the silicon substrate.

4.3 The surface carrier concentration, flatband capacitance, and flatband voltage, are computed from the capacitance and voltage data.

4.4 A voltage stress is applied to the sample at elevated temperature and the shift in V_{fb} is measured after cooling. This shift is interpreted as a measure of the concentration of mobile ionic charges in the oxide.



NOTE 1—Specimen exhibits permanent inversion layer.

FIG. 3 Capacitance-Voltage Plot of MOS Device Fabricated with *p*-Type Silicon

4.5 Total fixed-charge density is calculated from the flatband voltage.

4.6 The presence of subsurface P-N junctions is detected by photosensitivity. The specimen is biased into accumulation, and the capacitance measured and recorded. The specimen is then illuminated and the capacitance remeasured. An increase in capacitance due to illumination is interpreted as an indication of the presence of a P-N junction.

NOTE 1—Light will generate charge in the P-N junction and alter the capacitance of the junction which is in series with the MOS device. For the purposes of this test method, the subsurface region is defined as the region extending from the true surface to a depth at which no light penetrates. For the visible spectrum, maximum penetration depth is not well defined, as it depends on the intensity and spectral distribution of the light source and the carrier concentration of the silicon.

5. Significance and Use

5.1 Net carrier concentration present near the silicon-oxide interface may constitute an important acceptance requirement. Where there is not significant doping compensation by impurities of the opposite conductivity type, the material resistivity may be determined from this carrier concentration using Practice F 723.

5.2 Flatband voltage is an important parameter in the manufacture of MOS devices. Its value is dependent on the work function difference between the silicon and the metal field plate, interface trapped charge, and fixed or trapped charge distributed within the oxide. It can be an indicator of anomalies in these values **(4)**.

5.3 Instability of the flatband voltage of an MOS structure subjected to voltage stress at elevated temperatures is a measure of the mobile ionic charge concentration within the oxide. Most device applications require that mobile ionic charge be minimized.

5.4 This test method may be employed for qualification of furnaces or other semiconductor device-processing equipment where such qualification depends on the determination of contamination resulting from high mobile ionic charge concentration.

5.5 The presence of unwanted subsurface P-N junctions may have deleterious effects on device operation.

6. Interferences

6.1 If the apparatus is not well shielded from electromagnetic interference caused by radio frequency (r-f) fields, their presence may affect the measurements since the impedance of the MOS structure is high and since the test signal used is in the mV range.

6.2 The presence of any light during the measurements will adversely affect the results as the capacitance of the MOS device in the inversion condition is light sensitive.

6.3 The measurement may be affected if the relative humidity of the environment is permitted to exceed 60 %. The use of dry N_2 gas flowing into the sample chamber is recommended to control excess humidity.

6.4 The presence of a permanent surface inversion layer condition can affect the measurement.

NOTE 2—A permanent surface inversion layer condition makes it difficult to determine the value for C_{min} to be used in the calculations. If

an incorrect C_{min} were chosen, all shift values would still be correct, but doping and fixed charge computations would be wrong.

6.5 Stray capacitance and inductance caused by excessive lengths of connecting cable and by improper zeroing of the capacitance measuring instrument can cause significant errors in the capacitance measurement. Typical cable lengths should be kept below 1 m.

6.6 Alternating Current, (a-c) test signals greater than 25 mV rms can lead to errors in the measured capacitance.

6.7 Series resistance between the MOS capacitor and the capacitance measuring instrument can cause significant errors in the measured capacitance. Sources of series resistance can be in the sample itself, in the back contact, or in the test cables.

6.8 A leaky oxide which draws significant current can cause errors in the measured capacitance.

6.9 Inability of an inversion layer to form in an MOS sample will preclude measurement by this test method.

6.10 Very long minority-carrier lifetime in an MOS sample may cause errors in the measurement of C_{min} if the inversion layer has not had sufficient time to form.

NOTE 3—A maximum lifetime cannot be specified readily. However, an error will occur if the lamp in 11.9 is not illuminated for sufficient duration, or is not of sufficient intensity to generate charge to form the inversion layer.

6.11 Prolonged negative-bias temperature stressing can result in a shift in flatband voltage larger than the shift due to mobile ionic charge alone.

6.12 Hysteresis in the capacitance-voltage characteristics of an MOS sample can cause significant error in the determination of mobile ionic charge concentration.

7. Apparatus

7.1 *Facilities*, for growing gate quality oxides and for depositing and defining metal field plates on the oxide.

7.2 *Electrical Apparatus*:

7.2.1 *Ramping d-c Voltage Supply*, covering the range ±100 V and capable of sweeping between any two preset voltages within that range. Sweeping rate shall be variable between 0.1 and 1 V/s. Ripple shall be 0.5 % of the d-c output, or less. The supply shall be capable of supplying a fixed preset voltage with an accuracy of ±10 mV.

7.2.2 *Capacitance Meter*, with full scale ranges of 1 pF to 1000 pF, or greater, in decade, or smaller, steps. The measurement frequency shall be in the range 0.9 to 1.1 MHz inclusive. The accuracy shall be 0.5 % of full scale or better for each range and the reproducibility shall be 0.25 % of full scale or better. The instrument shall be capable of sustaining an external d-c bias of ±100 V or greater and shall be capable of compensating for an external probe fixture with stray capacitance of up to 5 pF. The a-c measuring signal shall be 0.025 V rms or less. The meter shall have an analog voltage output proportional to the capacitance measurement; output impedance shall be 100 Ω, or less.

NOTE 4—C-V measurements of MOS capacitors built from thin oxides on high resistivity substrates exhibit high series resistance effects which may require concurrent conductance measurements and subsequent computations to determine the true MOS capacitance. This test method is limited to capacitance-only measurements, but includes a test in 12.1 to check for the presence of series resistance effects.

7.2.3 *Digital Voltmeter (DVM)*, with sensitivity 1 µV or better, accuracy of 0.5 % of full scale or better, a reproducibility of 0.25 % of full scale or better, an input impedance of 10 MΩ or greater, and a common mode rejection 100 dB or greater at 60 Hz.

7.2.4 *X-Y Recorder*, with a minimum slewing speed of 20 cm/s, an accuracy of 0.5 % of full scale or better, a linearity of 0.5 % of full scale or better, and an input impedance of 1 MΩ or greater. *X*-axis and *y*-axis sensitivities shall be 5 mV/cm or greater.

7.2.5 *Stress Bias d-c Power Supply*, capable of supplying 0 to ±100 V (open circuit) with ripple 1 % of the d-c output or less, to be used for voltage stressing.

7.3 *Standard Capacitors*, of accuracy 0.25 % or better at the measurement frequency. At least one capacitor shall be used for each capacitance meter range used. At least one capacitor shall be in the range 1 to 10 pF inclusive and one shall be in the range 10 to 100 pF inclusive.

7.4 *Probe Fixture*:

7.4.1 *Probe*, to contact the top field plate; probe force shall not exceed 1.75 N; probe tip shall have a nominal radius of curvature of 5 µm; probe and holder should be designed such that the stray capacitance is less than 1 pF.

7.4.2 *Vacuum Chuck*, to hold the specimen wafer and contact the back surface; capable of reaching a temperature of 300°C, and maintaining set temperature to within ±10°C over the specimen area.

7.4.3 *Light Tight Metal Box*, to enclose the specimen during the measurement. Equipped with incandescent lamp, 7 to 20 W.

7.4.4 *Dry N_2 Gas Flow*, to control the humidity in the sample chamber.

7.5 *Equipment*, to measure the temperature of the vacuum chuck of 7.4.2 with an accuracy of ±2°C.

7.6 *Toolmaker's Microscope, Shadowgraph or Planimeter*, capable of measuring the field plate diameter to an accuracy of 0.5 % or better or the field plate area to an accuracy of 1 % or better.

7.7 *Shielded Cables*, for making electrical connections between the probe fixture, ramping voltage supply, capacitance meter, and digital voltmeter.

7.8 *Precision Voltage Source*, capable of providing output voltages from − 100 to + 100 V. The accuracy of this source shall be 0.1 % or better.

7.9 *A d-c Current Detector*, capable of measuring currents in the range from 100 nA to 1 mA, inclusive, with an accuracy of± 1 %.

NOTE 5—This test method indicates the use of basic analog instrumentation to perform the various test procedures. This does not preclude the implementation of this test method by computerized or otherwise automated instrumentation provided that such instrumentation is of equivalent accuracy and that the algorithms used therewith conform to the procedures of this test method.

8. Sampling

8.1 A specimen wafer sampling plan shall be agreed upon by all parties to the test. This sampling plan shall address the number of wafers per lot to be tested and the number of test points per wafer.

9. Test Specimen

9.1 Fabricate the MOS structure consisting of a silicon wafer covered by a layer of SiO_2, over which an array of metal field plates is deposited. Metallize the back surface of the wafer.

9.2 It is not necessary to remove oxide films, if they are present, from the back surface of an MOS wafer before deposition of metal on that surface, provided the wafer is larger than 5 cm^2 and that more than 90 % of the back surface is covered with metal.

NOTE 6—For relatively thick bulk wafers with resistivity greater than 10Ω· cm and thickness greater than 300 µm, the resistive component of the total impedance can become comparable to the capacitance component, depending on the oxide thickness and field plate area used. For these wafers it may be necessary to remove the back oxide before applying the back metal layer, or to reduce field plate area.

9.3 The metal field plate thickness shall be between 150 and 800 nm. The field plate area shall be less than or equal to 1 % of the area of the back contact. The field plate area and oxide thickness shall be chosen so that the maximum capacitance does not exceed 1000 pF, and the minimum is not less than 10 pF. Oxide thicknesses are typically between 50 and 300 nm.

10. Calibration

10.1 Connect shielded cables of a length suitable for measuring the standard capacitors (see 7.7) to the capacitance meter. Zero the capacitance meter with the cables connected to the meter but not to the standard capacitors.

10.2 Connect the cables to one of the standard capacitors. Select the range on the capacitance meter so that the capacitance indication does not exceed full scale. Measure and record the capacitance in pF. Measure and record the analog output voltage. Disconnect the cables from the capacitor. Determine the conversion factor between V and pF at the output of the capacitance meter. Repeat for each standard capacitor.

10.3 To verify that the digital voltmeter is within specification over the range from − 100 to + 100 V, inclusive, use it to measure the precision voltage source at five or more voltages in that range.

10.4 To verify that the *x-y* recorder is within specification, check deflection on both the *x*-axis and *y*-axis using the precision voltage source as an input source on suitable ranges. Using the conversion factors found in 10.2, the *y*-axis can be calibrated in terms of capacitance.

10.5 If either the capacitance meter, digital voltmeter, or *x-y* recorder is not within the required specification (see 7.2.2, 7.2.3 and 7.2.4 for values), make necessary adjustments in accordance with manufacturer's instructions to bring equipment to within specifications before proceeding with the measurement of the specimen.

11. Procedure

11.1 Measure and record the oxide thickness in nm in accordance with Test Method F 576 or Method F 388 or other appropriate means.

11.2 Measure and record the field plate area in cm^2.

11.3 Set all voltage supplies to zero output and connect all components in the manner shown in Fig. 4. Place the specimen wafer on the vacuum chuck and turn on the vacuum. Contact the field plate of one MOS device with the probe. Use sufficient probe pressure to ensure that a stable capacitance reading is obtained, but avoid probe force high enough to cause the probe to penetrate the oxide and cause shorting or leakage.

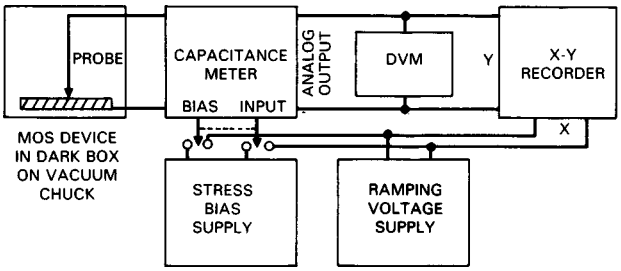


FIG. 4 Capacitance-Voltage Measurement Circuit

11.4 Bias the specimen with voltages of ±(*t*/10) V, where *t* is the measured oxide thickness in nm, and measure the current. A current of ±10 µA or more indicates a leaky device. If the specimen is leaky, do not proceed with the measurement since current flow indicates a defective oxide. Reduce the voltage to zero, lift the probe, and select another specimen.

NOTE 7—The critical dielectric field of 5 MV/cm is equivalent to 0.5 V/nm. The field used for the test in 11.4 is therefore 20 % of the critical field. A higher test field could be used, but is not necessary because the biases used in 11.4 are sufficient to achieve accumulation and inversion in applicable specimens.

11.5 Select the most sensitive range of the capacitance meter for which the indication does not go off scale. Raise the probe so that electrical contact to the field plate is just broken. Adjust the capacitance meter zero compensation control so that the indication on the selected range is 0 pF, within the accuracy of the instrument. Lower the probe and make contact again to the field plate.

11.6 Close the light tight box.

11.7 Set the sweeping power supply for voltage output of *t*/10V, where *t* is the measured oxide thickness in nm. Measure and note the capacitance indication. Set the sweeping power supply for a voltage output of − *t*/10V, where *t* is the measured oxide thickness in nm. Measure and note the capacitance indication. If the capacitance increases then the substrate is *p*-type. If the capacitance decreases, the substrate is *n*-type. Record the type determination.

11.8 *Determination of* C_{max}:

11.8.1 If the specimen substrate is *n*-type set the sweeping power supply for a voltage output of *t*/20V, where *t* is the measured oxide thickness in nm. Increase the voltage output in 5 V increments until the measured capacitance increment is less than 1 %. Record the measured capacitance as C_{max}. Record the voltage as V_{max}. If necessary, adjust the range of the capacitance meter so the indication does not exceed full scale.

11.8.2 If the specimen substrate is *p*-type set the sweeping power supply for a voltage output of − *t*/20V, where *t* is the measured oxide thickness in nm. Decrease the voltage output in 5 V increments (that is − *t*/20 − 5, − *t*/20 − 10, − *t*/20 − 15, etc.) until the measured capacitance increment is less than 1 %. Record the measured capacitance as C_{max}. Record the voltage as V_{max}. If necessary, adjust the range of the capacitance meter so the indication does not exceed full scale.

11.9 *Determination of* C_{min}:

11.9.1 If the specimen substrate is *n*-type:

11.9.1.1 Set the sweeping power supply for a voltage output of − *t*/20V, where *t* is the measured oxide thickness in nm. Turn on the lamp to illuminate the specimen. Decrease the voltage output in 5 V increments (that is − *t*/20 − 5, − *t*/20 − 10, − *t*/20 − 15, etc.) until the measured capacitance increment is less than 1 %.

11.9.1.2 Turn the lamp off. Note the capacitance indication. The capacitance indication will drop. Wait until the capacitance indication has stabilized within the accuracy of the instrument.

11.9.1.3 Record the measured capacitance as C_{min}. Record the voltage as V_{min}.

11.9.2 If the specimen substrate is *p*-type:

11.9.2.1 Set the sweeping power supply for a voltage output of *t*/20V, where *t* is the measured oxide thickness in nm. Turn on the lamp to illuminate the specimen. Increase the voltage output in 5 V increments until the measured capacitance increment is less than 1 %.

11.9.2.2 Turn the lamp off. Note the capacitance indication. The capacitance indication will drop. Wait until the capacitance indication has stabilized within the accuracy of the instrument.

11.9.2.3 Record the measured capacitance as C_{min}. Record the voltage as V_{min}.

11.10 Record the C-V plot as follows:

11.10.1 Prepare the sweeping power supply to sweep from V_{min} to V_{max}. The sweeping rate should be set to complete the sweep in a time period of approximately 60 s.

11.10.2 Set the range and sensitivity of the *x*-axis of the *x-y* recorder to record voltages between V_{min} and V_{max}. Set the range and sensitivity of the *y*-axis of the *x-y* recorder to plot voltages corresponding to capacitances ranging from 0 to C_{max} pF.

11.10.3 Set the sweeping power supply to apply a voltage of V_{min} to the sample.

11.10.4 Turn on the lamp to illuminate the specimen for 5 s.

11.10.5 Turn the lamp off. Note the capacitance indication. The capacitance indication will drop. Wait until the capacitance indication has stabilized within the accuracy of the instrument.

11.10.6 Activate the pen on the *x-y* recorder. Operate the sweeping power supply to generate the C-V plot. Lift the pen from the *x-y* recorder. Label the plot *I*.

11.10.7 To check for hysteresis, set the sweeping power supply to sweep from V_{max} to V_{min}. Activate the pen on the *x-y* recorder and operate the sweeping power supply to obtain a reverse C-V sweep. Lift the *x-y* recorder pen. Label the plot *R*.

11.11 Disconnect the sweeping power supply and apply the stress voltage supply. Set the stress voltage supply for *t*/10V, where *t* is the measured oxide thickness in nm.

11.12 Measure and record the temperature of the specimen.

11.13 Raise the specimen to a temperature of at least 200°C, but no more than 275°C for a time interval between 3 and 10 min. The time and temperature used shall be agreed upon by all parties to the test.

11.14 Cool the specimen to the temperature measured in 11.12. Maintain the stress voltage during cooling.

11.15 Disconnect the stress supply and connect the sweeping voltage supply. Record the C-V plot as in 11.10.1 to 11.10.6. Label the plot + .

11.16 Disconnect the sweeping power supply and apply the stress voltage supply. Set the stress voltage supply for − *t*/10V, where *t* is the measured oxide thickness in nm.

11.17 Repeat 11.13.

11.18 Repeat 11.14.

11.19 Repeat 11.15, but label the plot − .

11.20 Determine the presence of subsurface P-N junctions:

11.20.1 Apply bias V_{max} to the specimen.

11.20.2 Measure and record the capacitance, C_1, in pF.

11.20.3 Turn on the lamp to illuminate the specimen.

11.20.4 Measure and record the capacitance, C_2, in pF.

11.20.5 Interpret a measureable difference between the capacitance C_1 and C_2 within the accuracy of the capacitance meter as evidence of a subsurface P-N junction.

11.21 Set all voltage supplies to 0 V and raise the probe from the sample.

12. Calculation

12.1 Calculate and record the geometric capacitance of the MOS specimen using the equation:

$$C_g = 1 \times 10^{19}\, e_{ox}\, A/t_{ox} \tag{1}$$

where:

C_g = the geometric capacitance, pF,
e_{ox} = the dielectric permittivity of the oxide, 3.400×10^{-13} F/cm,
t_{ox} = the oxide thickness, nm, and
A = the field plate area, cm^2.

Compare C_g to C_{max}. If there is more than a 5 % difference then series resistance has distorted the measured capacitance and the measurements should be repeated after steps have been taken to lower the sample series resistance effects. Appropriate measures are thicker oxides, smaller specimen area, or lower silicon resistivity.

NOTE 8—The error in capacitance measurement arises because a sample having a series resistance capacitance (RC) is being measured by a capacitance meter which reads equivalent parallel capacitance. The error is not only due to series resistance but to the product of ωRC, angular frequency times series resistance times capacitance. Because of spreading resistance effects, the ωRC product is reduced by *reducing* sample size.

12.2 Determine the minimum depletion layer capacitance per unit area, C_s:

12.2.1 If the C-V plot exhibits the characteristics of a permanent inversion layer with a well defined capacitance minimum, C_i, (Fig. 3), then use C_i for the value of C_{min}.

12.2.2 Calculate and record C_s using the equation:

$$C_s = 1 \times 10^{-12}\, (C_{max}/A)/((C_{max}/C_{min}) - 1) \tag{2}$$

where:

C_s = the minimum depletion layer capacitance per unit area, F/cm^2,
C_{max} = the accumulation capacitance, pF,
C_{min} = the inversion capacitance, pF, and
A = the field plate area in cm^2.

12.3 Calculate and record the doping concentration, *N*, using the equation **(5)**:

$$\log_{10} N = 30.3258 + 1.68278 \log_{10} C_s - 0.03177 (\log_{10} C_s)^2 \tag{3}$$

where:
N = average dopant density in depletion region, cm $^{-3}$, and
C_s = the minimum depletion layer capacitance per unit area, F/cm ^{2}.

NOTE 9—(Eq 3) is an approximate solution for N as a function of C_s that is valid at room temperature. The accuracy of the approximation is within ±5 % of the exact solution of the room temperature equation:

$$N = 6.2415 \times 10^{29} C_s^2 (\ln(N) - 23.362) \quad (4)$$

which may be solved by iteration. The precision of the doping computed using Equation is adequate for this test method.

12.4 Calculate and record the flatband capacitance, C_{fb}, using the equations:

$$C_{scfb} = 0.044148\, A\, (N/T)^{\frac{1}{2}} \quad (5)$$

and

$$C_{fb} = C_{scfb} C_{max}/(C_{scfb} + C_{max}) \quad (6)$$

where:
C_{scfb} = capacitance of the space charge layer in the silicon, pF,
A = field plate area, cm ^{2},
C_{max} = accumulation capacitance, pF,
N = carrier concentration, cm $^{-3}$,
T = absolute temperature, °K, and
C_{fb} = the flatband capacitance, pF.

12.5 Draw a horizontal line on the C-V plots parallel to the *x*-axis and intersecting the *y*-axis at the capacitance, C_{fb}(see Fig. 5).

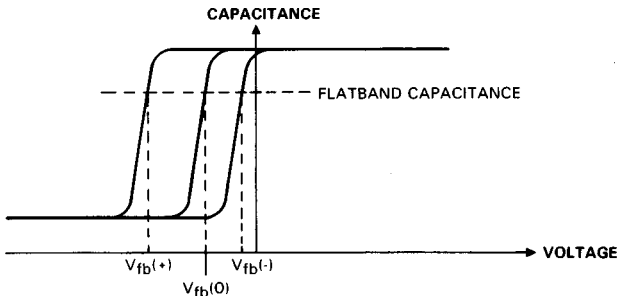
12.6 Locate the intersection of the horizontal line with the C-V plots:

12.6.1 Determine the voltage value at the intersection of the horizontal line with the C-V plot of 11.10 labelled *I*. Record this value as $V_{fb}(0)$.

12.6.2 Determine the voltage value at the intersection of the horizontal line with the C-V plot of 11.15 labelled + . Record this value as $V_{fb}(+)$.

12.6.3 Determine the voltage value at the intersection of the horizontal line with the C-V plot of 11.19 labeled − . Record this value as $V_{fb}(-)$.

12.7 Calculate the shifts in flatband voltage and corresponding mobile ionic charge concentrations:



NOTE 1—Horizontal line indicates flatband capacitance and its intersection with the C-V plots determines the flatband voltages.

FIG. 5 Capacitance-Voltage Plots of MOS Device Before and After Stress Cycles

12.7.1 Calculate and record the first flatband voltage shift, $\Delta V_{fb}(1)$, using the equation:

$$\Delta V_{fb}(1) = V_{fb}(+) - V_{fb}(0) \quad (7)$$

12.7.2 Calculate and record the second flatband voltage shift,$\Delta V_{fb}(2)$, using the equation:

$$\Delta V_{fb} = V_{fb}(-) - V_{fb}(+) \quad (8)$$

12.7.3 Calculate and record the mobile ionic charge concentration using the equation:

$$N_m = 6.2415 \times 10^6 \Delta V_{fb} C_{max}/A \quad (9)$$

where:
N_m = mobile ionic charge concentration, cm $^{-2}$,
ΔV_{fb} = the larger of [|g]D $V_{fb}(1)$[a]nd [|g]D $V_{fb}(2)$[f]latband voltage shifts calculated in equation Eq 7 and Eq 8, V,
C_{max} = accumulation capacitance, pF, and
A = device area, cm ^{2}.

NOTE 10—The flatband shift calculations are based on parallel displacements of the C-V curves of 11.10, 11.15, and 11.19. If these curves exhibit any distortions these may be an indication of poor contact, insufficient stress time or temperature, or change in interface trapped-charge density. The flatband shifts should be considered qualitative only.

12.8 Calculate and record the total fixed-charge density N_{tf} using these equations:

$$PB = 8.6173 \times 10^{-5} T (\ln(N) - 23.362) \quad (10)$$

Then, if *p*-type silicon use:

$$N_{tf} = 6.2415 \times 10^6 (C_{max}/A) \times (-VF - 4.7 + PM - PB) \quad (11)$$

or if *n*-type silicon use:

$$N_{tf} = 6.2415 \times 10^6 (C_{max}/A) \times (-VF - 4.7 + PM + PB) \quad (12)$$

where:
T = sample temperature, °K,
N = average doping concentration in depletion region, cm $^{-3}$,
PB = potential difference between fermi level and mid-gap, V,
N_{tf} = total fixed charge density, cm $^{-2}$,
VF = the most positive value from the measured $V_{fb}(0)$, $V_{fb}(+)$, and $V_{fb}(-)$, V,
C_{max} = accumulation capacitance, pF, and
PM = vacuum work function of gate metal (Aluminum = 4.2), V.

12.9 Determine the hysteresis in the C-V plot:

12.9.1 Draw a horizontal line on the C-V plots parallel to the *x*-axis and intersecting the *y*-axis at the capacitance, $(C_{min} + C_{max})/2$.

12.9.2 Locate the intersections of the horizontal line with the C-V plots of 11.10.6 and 11.10.7, labelled *I* and *R*, respectively.

12.9.3 Determine the absolute value of the voltage difference between the intersections. Record this value as V_h. A good

device will exhibit hysteresis less than the detectable limit, about 10 mV. Acceptable limits for hysteresis shall be agreed upon by all parties to the test.

13. Report

13.1 Report the following information:
13.1.1 Operator identification,
13.1.2 Date of measurement,
13.1.3 Lot number, wafer number, location of test MOS device on wafer, and device sampling plan if applicable,
13.1.4 Oxide thickness,
13.1.5 Oxide leakage current,
13.1.6 Device area, and if measured or calculated,
13.1.7 C_g,
13.1.8 C_{max}, C_{min}, and, if applicable, C_i,
13.1.9 V_{max} and V_{min},
13.1.10 Silicon type (N or P)
13.1.11 C_1 and C_2,
13.1.12 C_s,
13.1.13 N,
13.1.14 C_{fb},
13.1.15 $V_{fb}(0)$, $V_{fb}(+)$, and $V_{fb}(-)$,
13.1.16 $\Delta V_{fb}(1)$ andΔ $V_{fb}(2)$,
13.1.17 N_m,
13.1.18 N_{tf},
13.1.19 Stress voltage used,
13.1.20 Temperature of wafer before stress initiated,
13.1.21 Temperature of wafer during high temperature stress,
13.1.22 Duration of stress at high temperature, and
13.1.23 V_h.

14. Precision and Bias

14.1 Round robin experiments are being planned to determine the precision of this test method.

15. Keywords

15.1 capacitance-voltage; carrier concentration; fixed charge density; flatband capacitance; flatband voltage; metal-oxide-silicon structures; mobile ionic charge; MOS structures; silicon

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