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METRIC

Standard Practice for Determining Safe Current Pulse-Operating Regions for Metallization on Semiconductor Components [Metric][1]

This standard is issued under the fixed designation F 615M; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This practice covers procedures for determining operating regions that are safe from metallization burnout induced by current pulses of less than 1-s duration.

NOTE 1—In this practice, "metallization" refers to metallic layers on semiconductor components such as interconnect patterns on integrated circuits. The principles of the practice may, however, be extended to nearly any current-carrying path. The term "burnout" refers to either fusing or vaporization.

1.2 This practice is based on the application of unipolar rectangular current test pulses. An extrapolation technique is specified for mapping safe operating regions in the pulse-amplitude versus pulse-duration plane. A procedure is provided in Appendix X2 to relate safe operating regions established from rectangular pulse data to safe operating regions for arbitrary pulse shapes.

1.3 This practice is not intended to apply to metallization damage mechanisms other than fusing or vaporization induced by current pulses and, in particular, is not intended to apply to long-term mechanisms, such as metal migration.

1.4 This practice is not intended to determine the nature of any defect causing failure.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Terminology

2.1 *Definitions of Terms Specific to This Standard:*

2.1.1 *failure*—a change in the measured resistance of ± 10 % $\Delta R/R$ or as agreed upon by the parties to the test.

3. Summary of Practice

3.1 Specimens are selected from the population being evaluated.

3.2 The d-c resistance of each specimen is measured.

3.3 Each specimen is subjected to stress from rectangular current pulses varying in amplitude and duration according to a predetermined schedule of pulse width and amplitudes.

3.4 A second d-c resistance measurement is made on each specimen after each pulse, and it is characterized as having failed or survived.

3.5 The number, *x*, of specimens surviving and the total number, *n*, of specimens tested at each pulse width and amplitude are analyzed statistically to determine the burnout level at each test pulse width for the desired burnout survival probability and confidence level.

3.6 A point corresponding to the burnout level (at the desired probability and confidence level) is plotted for each of the test pulse duration values in the pulse-amplitude, pulse-duration plane. Based on these points, an extrapolation technique is used to plot the boundary of the safe operating region.

3.7 The following items are not specified by the practice and are subject to agreement by the parties to the test:

3.7.1 The procedure by which the specimens are to be selected.

3.7.2 Test patterns that will be representative of adjacent metallization on a die or wafer (5.3).

3.7.3 The schedule of pulse amplitudes and durations to be applied to the test samples (9.8).

3.7.4 The level of probability and confidence to be used in calculations to establish the boundary of the safe operating region (10.1).

3.7.5 The amount of change of resistance that will define the criterion for failure.

3.7.6 The statistical model to be used to determine the burnout probability at a desired stress level.

3.7.7 The form and content of the report.

[1] This practice is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

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4. Significance and Use

4.1 Solid-state electronic devices subjected to stresses from excessive current pulses sometimes fail because a portion of the metallization fuses or vaporizes (suffers burnout). Burnout susceptibility can vary significantly from component to component on a given wafer, regardless of design. This practice provides a procedure for establishing the limits of pulse current overstress within which the metallization of a given device should survive.

4.2 This practice can be used as a destructive test in a lot-sampling program to determine the boundaries of the safe operating region having desired survival probabilities and statistical confidence levels when appropriate sample quantities and statistical analyses are used.

NOTE 2—The practice may be extended to infer the survivability of untested metallization adjacent to the specimen metallization on a semiconductor die or wafer if care is taken that appropriate similarities exist in the design and fabrication variables.

5. Interferences

5.1 The level at which failure of metallization subjected to pulsed-current overstress occurs may be dependent on the temperature experienced by the semiconductor device. If significant differences in ambient temperature or heat sinking, or both, exist between one test situation and another, the results may not be representative.

NOTE 3—See Appendix X1 for a discussion of factors related to metallization heat sinking.

5.2 If probes are used to contact the metallization specimen, suitable precautions must be taken or the results may be misleading. The probes must not be allowed to come into contact with the area of metallization being characterized.

5.2.1 The use of Kelvin probe connections to make the resistance measurements is usually required to prevent contact resistance (at the current injection point) from interfering with the measurement.

5.2.2 Probe contacts with excessive contact resistance may cause damage at the point of contact. Such damage can interfere with the measurement.

5.3 If the test is used to infer the survivability of metallization on a wafer or die, the results could be misleading unless such factors as the following are identical: (*1*) metallization design geometry, (*2*) oxide step geometry, and (*3*) orientation of the metallization paths and oxide steps to the metallization source during deposition.

NOTE 4—The design and fabrication factors listed in 5.3 have been shown to be important for systems of aluminum metallization deposited on SiO_2/Si substrates. They are given as examples and are not intended to be all inclusive or necessarily to apply to all metallization systems to which this practice may be applied.

NOTE 5—Variations in oxide step geometry must be expected (see X1.4.2).

5.4 A step-stress pulsing schedule is not recommended. If such a schedule is used so that each specimen is subjected to successive pulses of increasing amplitude until failure occurs, the results could be misleading. It is possible that a pulse of the proper level can cause melting at a defect site without causing an open circuit; the molten metal may become redistributed so that the defect appears cured and will lead to failure on successive pulses.

6. Apparatus

6.1 *Current-Pulse Generator*—A source of rectangular current pulses capable of meeting the following requirements:

6.1.1 Risetime and falltime less than 10 % of the pulsewidth (full width at half maximum amplitude (FWHM)),

6.1.2 Impedance high enough with respect to the specimen metallization so that the pulse amplitude remains constant to within ±5 % between the end of the rise and beginning of the fall,

6.1.3 Jitter in the pulse amplitude and width less than ± 5 %,

6.1.4 Current amplitude and pulsewidth capability to provide pulses as agreed upon by the parties to the test, and

6.1.5 Single-pulse capability.

NOTE 6—Refer to Appendix X2 for information relating a rectangular pulse to an arbitrary pulse structure.

6.2 *Pulse-Monitoring Equipment*, as follows:

6.2.1 *Voltage-Monitoring Kelvin Probe*, for use in the circuit of Fig. 1, with risetime less than or equal to 5 % of the pulsewidth of the shortest pulse to be applied, and shunt capacitance sufficiently low so that the pulse shape is not distorted more than specified in 6.1:

6.2.2 *Voltage-Monitoring Resistor* (*R*, Fig. 1), with sufficiently low inductance, resistance, and shunt capacitance so that the generated pulse is not distorted more than specified in 6.1 and the value of the resistance is known within ±1 %.

6.2.3 *Current Probe*, for use in the circuit of Fig. 2, with risetime less than or equal to 5 % of the pulsewidth of the shortest pulse to be applied, with an ampere-second product sufficient to ensure nonsaturation for the amplitudes and durations of the pulses to be used and accurate within ±5 %.

6.3 *Pulse-Recording Equipment*, transient digitizer, oscilloscope with camera, storage oscilloscope, or other pulse recording means having a risetime less than 5 % of the width of the shortest test pulse used and capable of recording individual test pulses.

6.4 *Test Fixture*, providing means for the current pulse to be transmitted through the metallization specimen as well as through an equivalent resistance (see 9.5) without distortion of the pulse shape beyond that specified in 6.1. The test fixture must also provide a means for connecting the metallization specimen to the resistance-measuring equipment (see 6.5). The test fixture will contact the specimen through either standard component package leads or wafer probes. More than one test fixture may be used.

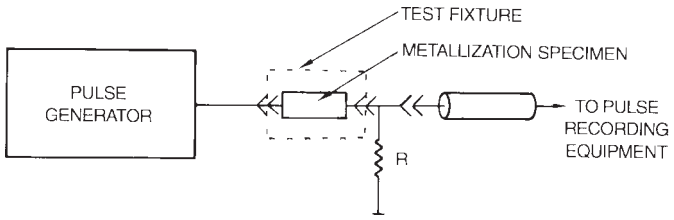


FIG. 1 Pulsing Circuit Using Resistor Voltage Drop to Monitor Current Through Specimen

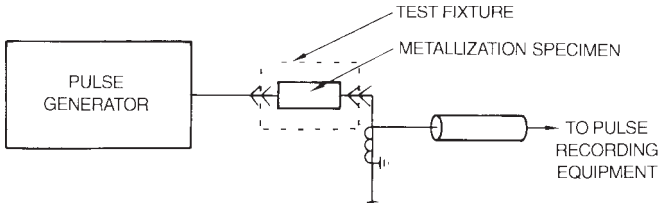


FIG. 2 Pulsing Circuit Using Current Probe to Monitor Current Through Specimen

6.5 *Resistance-Measuring Equipment*—A curve tracer, ohmmeter, or other means to be used for evaluating the d-c resistance and continuity of the current path on the specimen. The current through the specimen during this measurement should be minimized (less than 10 % of the d-c current rating of the specimen).

6.6 *Miscellaneous Circuit Components*, to be used as required in each of the test circuits (see Fig. 1 or Fig. 2). The switches, leads, and connections shall be of a quality used customarily in electronic circuit testing.

6.7 *Resistors*, as required, to match the d-c resistance of the unstressed specimen to within ±5 %.

7. Sampling

7.1 The procedure by which the sample is to be taken and the number of specimens for each test condition are not specified by this practice and are to be agreed upon by the parties to the test.

8. Test Specimen

8.1 The specimen may be an integrated circuit or a special test structure for the evaluation of a design or process, depending on the purpose for which the measurements are to be used.

9. Procedure

9.1 Assemble the pulsing circuit shown in either Fig. 1 or Fig. 2, so that a specimen can be connected via a suitable test fixture into the test circuit.

9.2 Turn on all equipment, and allow the apparatus to warm up in accordance with the manufacturer's instructions.

9.3 Connect the specimen to a suitable test fixture to measure the resistance of the specimen. If probes are used to contact the specimen, see 5.2 for precautions.

NOTE 7—Appropriate handling precautions must be taken to prevent electrostatic damage.

9.4 Measure and record the specimen resistance, in ohms or continuity, as required.

9.5 Connect an equivalent resistance into the pulse testing circuit and, by applying pulses through this resistor, establish and record the pulser settings required to generate the pulse amplitudes to be applied to the specimen and the appropriate settings for the pulse-monitoring equipment.

9.6 Connect the specimen into the pulsing circuit.

9.7 Set the current pulse generator and pulse monitoring equipment for a pulse of the designated amplitude and duration in accordance with the information recorded in 9.5.

9.8 Apply a single pulse of the scheduled amplitude and duration to the specimen.

9.9 Measure and record the specimen resistance (see 9.3 and 9.4).

9.10 Compare the value recorded in 9.9 with that recorded in 9.4. Characterize the specimen as failed if the resistance of the specimen has increased by the amount agreed upon by the parties to the test. Otherwise, characterize the specimen as survived. Record the characterization.

9.11 Repeat 9.3 through 9.10 for each specimen in the sample at each of the scheduled pulse amplitudes and durations, and record the number failing, $x_{\tau I}$, and the number tested, $n_{\tau I}$, at each pulse amplitude and duration.

10. Calculation and Interpretation of Results

10.1 Determine the safe operating region for general pulse duration, t, as indicated by Fig. 3. For each data point (τ, I), a safe operating region includes all points falling below the curve $I_s(t)$ as follows:

$$I_s(t) = I_\tau \sqrt{\frac{\tau}{t}}, t \geq \tau$$

where:

τ = test pulse width.

10.2 If more than one data point (τ, I_τ) has been established, the upper bound of the safe operating region is defined by the smallest value of $I_s(t)$ at any t as defined by all data points.

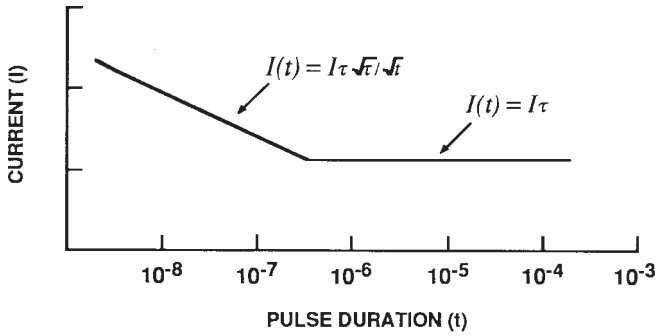
NOTE 8—See Appendix X2 for a method of extending these results to arbitrary pulse shape.

11. Report

11.1 The contents of the test report will vary depending on the purpose of the test. The specific format and content for the report (including the specific format in which the safe-operating area data is presented) are to be agreed upon by the parties to the test prior to the start of the test program.

12. Keywords

12.1 current pulse; current pulse burnout; metallization burnout; safe current pulse; semiconductor burnout



NOTE 1—The safe operating region is that region of the I, t plane below the solid boundary line.

FIG. 3 Example of a Safe Operating Region

APPENDIXES

(Nonmandatory Information)

X1. METALLIZATION BURNOUT MECHANISMS

X1.1 Scope

X1.1.1 This appendix describes the mechanisms involved in metallization burnout, as addressed in the practice. This practice deals with burnout failures that occur as the result of current pulses of less than 1-s duration.

X1.1.2 When metal interconnections on semiconductor components (semiconductor metallization) are damaged by current pulses of such duration, the damage is generally a result of resistive heating in the metallization (often at defect sites), which causes the metallization to melt, vaporize, or both. Semiconductor metallization can also burn out as a secondary result of heating in the underlying semiconductor material. This practice and the following discussion are aimed at mechanisms associated with resistive heating in the metallization. The practice is intended to define safe operating regions in which such failures will not occur and is not intended to determine the nature of any defect causing failure.

X1.2 Equations of Resistive Heating

X1.2.1 When an electrically resistive material is subjected to an electrical current, the differential equation for temperature rise at any point x is as follows:

$$Dc(T)\frac{dT}{dt} = J^2(x, t)\,p(T) - \frac{\partial H}{\partial t}(x, t) \qquad \text{(X1.1)}$$

where:

T = temperature,
D = density of the material,
$c(T)$ = temperature-dependent specific heat of the material,
$\rho(T)$ = temperature-dependent resistivity of the material,
$J(x, t)$ = time-dependent current density at position x, and
$\partial H/\partial t\,(x, t)$ = rate of thermal energy loss per unit mass from an increment of material at position x.

Any self-consistent set of units may be used.

X1.2.2 The term $\partial H/\partial t$ is dependent on the particular geometry, material, and ambient conditions. For general considerations, it is of interest to analyze the adiabatic case. In that case, $\partial H/\partial t$ is negligible and (Eq X1.1) can be rearranged and integrated directly as follows:

$$\int_{T_1}^{T_2} \frac{c(T)}{\rho(T)}\,dT = \int_{t_1}^{t_2} J^2(x, t)dt \qquad \text{(X1.2)}$$

where:

$T_2 - T_1$ = temperature rise at x caused by current flow in the time period t_1 to t_2.

X1.3 Calculation of Adiabatic Time Dependence for Melting in Aluminum

X1.3.1 For aluminum metallization, the functions $c\,(T)$ and $\rho(T)$ are approximately linear and of the form $y = mx + b$, where the parameters m and b can be determined from data such as those given in the *Handbook of Chemistry and Physics*. [2]

X1.3.1.1 Thus, for aluminum heated from room temperature (~22°C) to the melting temperature during the interval t_1 to t_2, (Eq X1.2) becomes as follows:

$$\int_{t_1}^{t_2} J^2(x, t)dt = 2.3 \times 10^8\ A^2{\cdot}\text{s/cm}^4 \qquad \text{(X1.3)}$$

X1.3.1.2 To melt the aluminum, the heat of fusion must be added during a time interval t_2 to t_3. Using the heat of fusion from the *Handbook of Chemistry and Physics*, [2] we can write as follows:

$$\int_{t_2}^{t_3} J^2(x, t)dt = 0.92 \times 10^8\ A^2{\cdot}\text{s/cm}^4 \qquad \text{(X1.4)}$$

$$\int_{t_1}^{t_3} J^2(x, t)dt = 3.2 \times 10^8\ A^2{\cdot}\text{s/cm}^4 \qquad \text{(X1.5)}$$

X1.3.2 For a square pulse of current I and duration τ_ρ through a metallization strip of cross-sectional area A, the current density required to cause complete melting in the adiabatic case is then as follows:

$$I/A = 1.8 \times 10^4\ \tau_p^{-1/2}\ A/\text{cm}^2 \qquad \text{(X1.6)}$$

X1.4 Discussion of General Time Dependence

X1.4.1 From the results of the preceding calculations, we see that the failure current has a $\tau^{-1/2}$ dependence in the adiabatic case. For a metallization strip of uniform cross section deposited on a planar substrate such as the common SiO_2/Si semiconductor construction, the adiabatic condition is applicable for pulse durations much less than the characteristic thermal relaxation time τ_c, which is given as follows:

$$\tau_c = \frac{cmx}{K} \qquad \text{(X1.7)}$$

where:

c = specific heat of the metallization,
m = mass per unit area of the metallization,
x = thickness of the layer between the metallization and its heat sink, and
K = thermal conductivity of the layer between the metallization and its heat sink.

Typical values of τ_c for such a system are of the order of 1 μs.

[2] The 42nd edition is available from the Chemical Rubber Publishing Co., Cleveland, OH, 1960.

X1.4.2 For a metallization strip containing points of reduced cross section, melting occurs first at the smallest cross-section site having $\tau_c \geq \tau_p$. An example of such a defect, which typically occurs in semiconductor components, is thin metal over an oxide step outlining a junction diffusion. Such defects are generally so narrow that $\partial H/\partial t$ is controlled by heat flow from the site to the surrounding metallization.

X2. EXTENSION OF RECTANGULAR CURRENT PULSE DATA TO THE ANALYSIS OF ARBITRARY CURRENT PULSE DATA FOR CAUSING METALLIZATION BURNOUT

X2.1 A useful method for relating rectangular pulse burnout data to arbitrary pulse shapes has been developed by Tasca, et al. [3] In that method, a convolution integral is formed involving arbitrary pulse power waveforms and the dependence of square pulse power on pulse duration. For metallization burnout, where purely resistive heating is involved, the method is approximately applicable with current substituted for power. The desired safe pulse amplitude for any pulse waveform $I_A(\tau)$ is then defined as follows:

$$1 > \int_O^{\tau_A} I_A^2(\lambda)\left\{\frac{d}{d(\tau - \lambda)}\left[\frac{1}{I_s^2\,(\tau - \lambda)}\right]\right\} d\lambda \qquad \text{(X2.1)}$$

where:

$I_s\,(t)$ = rectangular pulse current required to cause burnout,
τ_A = time to failure from a pulse of arbitrary form $I_A\,(t)$, and
λ = a dummy variable for integration purposes.

[3] Tasca, D. M., Peden, J. C., and Andrews, J. L., "Theoretical and Experimental Studies of Semiconductor Device Degradation Due to High Power Electrical Transients," *General Electric Document No. 735D4289*, December 1972, as Acquisition No. 20212 from FCDNA, Attn: DASIAC, 1680 Texas St., SE, Kirtland AFB, NM 87117.